REMARKS

Claims 21-27 are pending in the present application. Replacement claims 21-23 have been presented herewith. Also, claims 24-27 have been presented herewith.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119 and receipt of the priority document in parent application Serial No. 08/959,667.

Drawings

Applicant notes the Examiner's acceptance of the drawings as filed along with the present application on August 3, 2001.

Claim Rejections-35 U.S.C. 102

Claims 21-23 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Yamada et al. reference (U.S. Patent No. 5,864,178). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method for fabricating a semiconductor apparatus of claim 21 includes in combination fabricating a semiconductor substrate having a first surface in which a semiconductor integrated circuit is formed, "the semiconductor substrate including a conductive layer formed on the first surface thereof which is connected to the

semiconductor integrated circuit and including a base member of insulating material arranged between the first surface and the conductive layer, the base member including a first surface facing the first surface of the semiconductor substrate and a second surface opposite the first surface of the base member, the conductive layer having an extended portion extending on the second surface of the base member". The method further comprises "connecting the extended portion of the conductive layer to the connection substrate". Applicant respectfully submits that the Yamada et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has relied upon Figs. 56A-57 as described in columns 56-58 of the Yamada et al. reference as disclosing the features of claim 21. The Examiner has interpreted first encapsulation resin 204 of the Yamada et al. reference as the base member of claim 21, and bump electrode 203 as the conductive layer.

However, bump electrode 203 as illustrated in Fig. 56A of the Yamada et al. reference is formed directly on barrier metal layer 225. Barrier metal layer 225 is directly formed on bonding pad 224. Bump electrode 203 in Fig. 56A of the Yamada et al. reference is not formed on first encapsulation resin 204. Accordingly, semiconductor chip 201 in Fig. 56A of the Yamada et al. reference does not include a conductive layer and a base member formed on a first surface of a semiconductor substrate, wherein the conductive layer has an extended portion that extends on a second surface of the base member. That is, bump electrode 203 of the Yamada et al. reference is formed on barrier metal layer 225 and does not include an extended portion that extends on

first encapsulation resin 204, as would be necessary to meet the features of claim 21.

Since semiconductor chip 201 of the Yamada et al. reference does not include an extended portion of a conductive layer as featured in claim 21, the Yamada et al. reference clearly fails to disclose a method for fabricating a semiconductor apparatus including in combination "connecting the extended portion of the conductive layer to the connection substrate". Applicant therefore respectfully submits that the method for fabricating a semiconductor apparatus of claim 21 distinguishes over the Yamada et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 21-23, is improper for at least these reasons.

Claim 23, as dependent upon claim 21, further features that the base member and the seal member "are made of a same material having a same thermal expansion coefficient". Applicant respectfully submits that the Yamada et al. reference as relied upon by the Examiner does not disclose these features.

As noted above, the Examiner has interpreted first encapsulation resin 204 in Fig. 56A of the Yamada et al. reference as the base member of claim 21, and has further interpreted third encapsulation resin 206 as the seal member. However, as described in column 56, lines 29-48 of the Yamada et al. reference, the coefficient of thermal expansion of first encapsulation resin 204 is 40×10^{-6} ($°C^{-1}$). As further described in column 57, lines 24-31 of the Yamada et al. reference, the coefficient of thermal expansion of third encapsulation resin 206 is 30×10^{-6} ($°C^{-1}$). Accordingly, the thermal expansion coefficients of first and third encapsulation resins 204 and 206 of the

Yamada et al. reference are not the same, as would be necessary to meet the features of claim 23. The Yamada et al. reference as relied upon by the Examiner therefore fails to disclose a method for fabricating a semiconductor apparatus wherein a base member of a semiconductor substrate has a same thermal expansion coefficient as a seal member, and thus does not provide a semiconductor apparatus having reduced stress and distortion as in the present application. Applicant therefore respectfully submits that the method of claim 23 distinguishes over the Yamada et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 23, is improper for at least these additional reasons.

Claims 24-27

Applicant respectfully submits that claim 24, as dependent upon claim 21, distinguishes over and would not have been obvious in view of the prior art as relied upon by the Examiner, at least by virtue of dependency upon claim 21 and by further reason of the features therein.

Applicant also respectfully submits that the method for fabricating a semiconductor apparatus of claim 25 distinguishes over the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above. The Yamada et al. reference as relied upon by the Examiner does not disclose forming a base member on a first surface of a semiconductor substrate; forming a conductive layer on the first surface of the semiconductor substrate, "the conductive layer being connected to the

semiconductor integrated circuit and having an extended portion that extends onto a top surface of the base member"; and connecting the extended portion of the conductive layer to the connection substrate. That is, bump electrode 203 in Fig. 56A of the Yamada et al. reference is formed on barrier metal layer 225, and does not include an extended portion which extends onto a top surface of first encapsulation resin 204, as would be necessary to meet the features of claim 25. Accordingly, Applicant respectfully submits that claims 25-27 distinguish over the Yamada et al. reference as relied upon by the Examiner for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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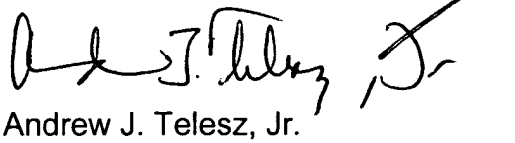

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Enclosures: Version with Marked-Up Changes

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Claims:

21. (Twice Amended) A method for fabricating a semiconductor apparatus, comprising:

fabricating a semiconductor substrate having a first surface in which [comprises] a semiconductor integrated circuit is formed,

the semiconductor substrate including a conductive layer formed on the first surface thereof which is connected to the semiconductor integrated circuit and including[, and an electrode, which is composed of] a base member of insulating material arranged between the first surface and the conductive layer,

the base member including a first surface facing the first surface of the semiconductor substrate and a second surface opposite the first surface of the base member,

the [formed on the semiconductor integrated circuit and a] conductive layer having an extended portion extending [formed] on the second surface of the base member;

providing a connection substrate on which the semiconductor substrate is to be mounted;

placing the semiconductor substrate so that the first surface of the semiconductor substrate faces the [to face a] connection substrate;

connecting the extended portion of the conductive layer [electrode] to the

connection substrate; and

supplying a seal member in a [the] space between the semiconductor substrate and the connection substrate.

22. (Amended) A method according to claim 21, wherein the first surface of the semiconductor substrate is placed to face the connection substrate using [according to] a face down technique.

23. (Amended) A method according to claim 21, wherein the base member and the seal member are made of [the] a same material having a same thermal expansion coefficient.